UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,734	08/04/2003	Antti Kiiveri	915-008.012	6648

4955 7590 10/15/2010

WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
PERUNGAVOOR, VENKATANARAY	
ART UNIT	PAPER NUMBER
2432	
MAIL DATE	DELIVERY MODE
10/15/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/634,734	KIIVERI ET AL.	
	Examiner	Art Unit	
	Venkat Perungavoor	2432	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/29/2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-14 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,4-8,10-14,16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/29/2010 has been entered.

Response to Arguments

Applicant's arguments, see pages 6-9, filed 7/29/2010, with respect to the rejection(s) of claim(s) 1-2,4-8,10-13,15-18 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of US Patent Pub 2002/0184523 to Barrenscheen and US Patent Pub 2002/01660632 to Helbig Sr.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2, 4-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-2, 4-6 recite elements that are a means (or step) plus function limitation that invoke 35 U.S.C. 112, sixth paragraph. However, the written description fails to clearly link or associate the disclosed structure, material, or acts to the claimed function such that one of ordinary skill in the art would recognize what structure, material, or acts perform the claimed function. The claim does not provide details to the structure of each of the means, e.g. what structure corresponds to storage circuit access control means?

For a computer-implemented means-plus-function claim limitation that invokes 35 U.S.C. 112, sixth paragraph, the corresponding structure is required to be more than simply a general purpose computer or microprocessor. The corresponding structure for a computer-implemented function must include the algorithm as well as the general purpose computer or microprocessor, i.e. the algorithm should be identified.

Applicant is required to:

(a) Amend the claim so that the claim limitation will no longer be a means (or step) plus function limitation under 35 U.S.C. 112, sixth paragraph; or

(b) Amend the written description of the specification such that it clearly links or associates the corresponding structure, material, or acts to the claimed function without introducing any new matter (35 U.S.C. 132(a)); or

(c) State on the record where the corresponding structure, material, or acts are set forth in the written description of the specification that perform the claimed function. For more information, see 37 CFR 1.75(d) and MPEP §§ 608.01(o) and 2181.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-8, 10-14 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Pub 2002/0184523 to Barrenscheen in view of US Patent Pub 2002/0166062 to Helbig Sr.

Regarding Claim 1, Barrenscheen discloses Circuitry for providing data security, which circuitry contains at least one processor, at least one storage circuit, authentication means arranged to authenticate software provided to the circuitry, and which circuitry comprises:

at least one storage area in said storage circuit, in which storage area protected data relating to security functions of the circuitry and protected applications are located see Par. 0016;

mode setting means arranged to set said processor in one of at least two different operating modes, the mode setting means being capable of altering the processor operating mode see Par. 0071;

storage circuit access control means arranged to enable said processor to access said storage area in which said protected data are located when a first processor operating mode is set see par. 0066 & Par. 0062; and

storage circuit access control means arranged to prevent said processor from accessing said storage area in which said protected data are located when a second processor operating mode is set, thereby enabling said at least one processor to execute non-verified software downloaded into the circuitry, wherein said second processor operating mode is set when testing or debugging is performed see Par. 0065 & Par. 0059 & Par. 009.

But Barrenscheen does not disclose the authentication of software. However, Helbig discloses the only authenticated software authenticated by said authentication means and said protected applications have access to said protected data see Par. 0016.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the authentication of software in the invention of Barrenscheen in order to have thwart attacks and corruption of sensitive data as taught in Helbig see Par. 008.

Regarding Claim 2, 8, 14, Barrenscheen does not discloses the timer. However, Heilbig discloses The circuitry for providing data security according to claim 1, further comprising:

a timer arranged to control a time period during which the processor is in said second operating mode see Par. 0150.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include a timer in the invention of Barrenscheen in order to have state like process for different modes as taught in Helbig see Par. 0057.

Regarding Claim 4. 10, 16, Barrenscheen discloses The circuitry for providing data security according to claim 1, further comprising: means arranged to indicate in which mode the processor is operating see Par.. 0061.

Regarding Claim 5. 11, 17, Barrenscheen discloses The circuitry for providing data security according to claim 1, wherein said
mode setting means comprise an application program see Par. 0052.

Regarding Claim 6. 12, 18, Barrenscheen discloses The circuitry for providing data security according to claim 1, which circuitry is comprised in a mobile telecommunication terminal see Par. 009.

Regarding Claim 7. Barrenscheen discloses A method, comprising:

storing protected data relating to security functions of circuitry and protected applications in a storage circuit see Par. 0016;
setting a processor in one of at least two different alterable operating modes see Par.

0055-0059;

enabling said processor to access said storage area in which said protected data are located when a first processor operating mode is set see par. 0066 & Par. 0062; and

preventing said processor from accessing said storage area in which said protected data are located when a second processor operating mode is set, thereby enabling said at least one processor to execute non-verified software downloaded into the circuitry, wherein said second processor operating mode is set when testing or debugging is performed see Par. 0065 & Par. 0059 & Par. 009.

But Barrenscheen does not disclose the authentication of software. However, Helbig discloses the only authenticated software authenticated by said authentication means and said protected applications have access to said protected data see Par. 0016.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the authentication of software in the invention of Barrenscheen in order to have thwart attacks and corruption of sensitive data as taught in Helbig see Par. 008.

Regarding Claim 13. Barrenscheen discloses Data security circuitry for providing data security, which data security circuitry contains at least one processor, at least one storage circuit, authentication circuitry arranged to authenticate software provided to the data security circuitry and which data security circuitry comprises:

at least one storage area in said storage circuit, in which storage area protected data relating to security functions of said data security circuitry and protected applications are located see Par. 0016 ;

mode setting circuitry arranged to set said processor in one of at least two different operating modes, the mode setting circuitry being capable of altering the processor operating mode see Par. 0055-0059;

storage circuit access control circuitry arranged to enable said processor to access said storage area in which said protected data are located when a first processor operating mode is set see par. 0066 & Par. 0062; and

storage circuit access control circuitry arranged to prevent said processor from accessing said storage area in which said protected data are located when a second processor operating mode is set, thereby enabling said at least one processor to execute non-verified software downloaded into the data security circuitry for providing data security, wherein said second processor operating mode is set when testing or debugging is performed see Par. 0065 & Par. 0059 & Par. 009.

But Barrenscheen does not disclose the authentication of software. However, Helbig discloses the only authenticated software authenticated by said authentication means and said protected applications have access to said protected data see Par. 0016.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the authentication of software in the invention of Barrenscheen in

order to have thwart attacks and corruption of sensitive data as taught in Helbig see Par. 008.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Venkat Perungavoor whose telephone number is (571)272-7213. The examiner can normally be reached on 8:00-4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/V. P./
Examiner, Art Unit 2432
10/8/10

/Minh Dinh/
Primary Examiner, Art Unit 2432